WHAT IS CLAIMED IS:

1. An EEPROM cell formed on a substrate having an outer surface, comprising:

first and second conductive regions in the substrate below the substrate's outer surface, the first and second conductive regions are laterally displaced from one another by a predetermined distance;

an insulating layer outwardly from the outer surface of the substrate, the insulating layer positioned so that its edges are substantially in alignment between the first and second conductive regions;

a floating gate layer outwardly from the insulating layer and in substantially the same shape as the insulating layer; and

a diffusion region that extends laterally from at least one of the first and second conductive regions so as to overlap with the insulating layer, the diffusion region is operable to provide a source of charge for placement on the floating gate layer when programming the EEPROM cell.

2. The EEPROM cell of Claim 1 wherein the diffusion region further comprises a first diffusion region that extends laterally from the first conductive region so as to overlap with the insulating layer and a second diffusion region that extends laterally from the second conductive region so as to overlap with the insulating layer.

3. The EEPROM cell of Claim 1 wherein the insulating layer is formed from oxide.

4. The EEPROM cell of Claim 1 wherein the floating gate layer is formed from polysilicon.

5. The EEPROM cell of Claim 1 wherein the floating gate layer and insulating layers are patterned on the surface of the substrate so as to increase the edge length of the floating gate layer and insulating layer with respect to the first and second conductive regions.

6. The EEPROM cell of Claim 5 wherein the pattern of the floating gate and insulating layers is a snake pattern.

7. The EEPROM cell of Claim 5 wherein the pattern of the floating gate and insulating layers is a comb pattern.

8. The EEPROM cell of Claim 5 wherein the pattern of the floating gate and insulating layers is a fishbone pattern.

9. The EEPROM cell of Claim 5 wherein the pattern of the floating gate and insulating layers is a waffle pattern.

10. The EEPROM cell of Claim 1 wherein the first and second conductive regions are heavy doped N+ regions on the order of 1×10^{16} to $1 \times 10^{18} cm^{-3}$.

11. A method for forming an EEPROM cell on a substrate having an outer surface, the method comprising the steps of:

forming first and second conductive regions in the substrate below the substrate's outer surface, the first and second conductive regions are laterally displaced from one another by a predetermined distance;

forming an insulating layer outwardly from the outer surface of the substrate, the insulating layer positioned so that its edges are substantially in alignment between the first and second conductive regions;

forming a floating gate layer outwardly from the insulating layer and in substantially the same shape as the insulating layer; and

forming a diffusion region that extends laterally from at least one of the first and second conductive regions so as to overlap with the insulating layer, the diffusion region is operable to provide a source of charge for placement charge on the floating gate layer when programming the EEPROM cell.

12. The method of Claim 11 wherein the forming a diffusion region step further comprises forming a first diffusion region that extends laterally from the first conductive region so as to overlap with the insulating layer and forming a second diffusion region that extends laterally from the second conductive region so as to overlap with the insulating layer.

13. The method of Claim 11 wherein the insulating layer is formed from oxide.

14. The method of Claim 11 wherein the floating gate layer is formed from polysilicon.

15. The method of Claim 11 wherein the forming the floating gate layer and insulating layers steps further comprises patterning the layers on the surface of the substrate so as to increase the edge length of the floating gate layer and insulating layer with respect to the first and second conductive regions.

16. The method of Claim 15 wherein the pattern of the floating gate and insulating layers is a snake pattern.

17. The method of Claim 15 wherein the pattern of the floating gate and insulating layers is a comb pattern.

18. The method of Claim 15 wherein the pattern of the floating gate and insulating layers is a fishbone pattern.

19. The method of Claim 15 wherein the pattern of the floating gate and insulating layers is a waffle pattern.

20. The method of Claim 11 wherein the first and second conductive regions are formed from heavy doped N+ material on the order of 1×10^{16} to $1 \times 10^{18} cm^{-3}$.

21. An EEPROM cell formed on a substrate having an outer surface, comprising:

a deep conductive region in the substrate below the substrate's outer surface;

first and second conductive regions in the substrate below the substrate's outer surface, the first and second conductive regions are laterally displaced from one another by a predetermined distance;

an insulating layer outwardly from the outer surface of the substrate, the insulating layer positioned so that its edges are substantially in alignment between the first and second conductive regions;

a floating gate layer outwardly from the insulating layer and in substantially the same shape as the insulating layer; and

wherein the deep conductive region is operable to provide a source of charge for placement on the floating gate layer when programming the EEPROM cell.

22. The EEPROM cell of Claim 21 wherein the insulating layer is formed from oxide.

23. The EEPROM cell of Claim 21 wherein the floating gate layer is formed from polysilicon.

24. The EEPROM cell of Claim 21 wherein the deep conductive region is doped N+ on the order of 1×10^{16} cm^{-3}.

25. A method for forming EEPROM cell on a substrate having an outer surface, the method comprising the steps of:

forming a deep conductive region in the substrate below the substrate's outer surface;

forming first and second conductive regions in the substrate below the substrate's outer surface, the first and second conductive regions are laterally displaced from one another by a predetermined distance;

forming an insulating layer outwardly from the outer surface of the substrate, the insulating layer positioned so that its edges are substantially in alignment between the first and second conductive regions;

forming a floating gate layer outwardly from the insulating layer and in substantially the same shape as the insulating layer; and

wherein the deep conductive region is operable to provide a source of charge for placement on the floating gate layer when programming the EEPROM cell.

26. The method of Claim 25 wherein the insulating layer is formed from oxide.

27. The method of Claim 25 wherein the floating gate layer is formed from polysilicon.

28. The method of Claim 25 wherein the deep conductive region is doped N+ on the order of 1×10^{16} cm^{-3}.